REMARKS

At the time the current Official Action was mailed, claims 1-20 were pending. In the Office Action, the Examiner objected to claims 2-7 and indicated that claims 2-7 would be allowable if rewritten in independent form. Applicants thank the Examiner for indicating the allowable subject matter of claims 2-7. Further, the Examiner rejected claims 1 and 8-20. By the present Response, Applicants amend claim 9 to correct a clerical error. Reconsideration of the application in view of the remarks set forth below is respectfully requested.

As a preliminary matter, Applicants would like to point out that the PTOL-326 form submitted with the Official Action *again* indicates that claims 1-20 are subject to restriction and/or election requirement. This point was not addressed by the Examiner in the Official Action. Applicants assume that the indication of the restriction requirement was made inadvertently, and therefore, have made no election. If this assumption is incorrect, Applicants respectfully request that the Examiner specify which claims are subject to restriction/election. Applicants respectfully submit that no restriction and/or election is required in the instant case.

Objections to the claims

The Examiner objected to claims 2-7 as being dependent upon a rejected base claim and indicated that claims 2-7 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants thank the Examiner for the indication of allowability of the subject matter separately recited in each of claims 2-7. However, Applicants respectfully submit that claims 2-7 are also allowable based on their dependency to allowable base claim 1. For the reasons set forth below with respect to the rejection of

independent claim 1 under 35 U.S.C. § 102, Applicants respectfully submit that claims 2-7 are currently in condition for allowance, without amendment.

Rejections under 35 U.S.C. § 102

The Examiner rejected claims 1, 9-11, 15, 18, and 20 under 35 U.S.C. § 102 as being anticipated by Blackshear et al. (U.S. Patent No. 6,774,475 B2; hereinafter "Blackshear"). Specifically, the Examiner stated:

> Blackshear teaches all of the positive steps of claims 1, 9-11, 15, 18, and 20 in that a stack of at least two semiconductor die are formed (column 4 lines 8-9), and the stack is tested prior to mounting on a packaging substrate (claim 14).

Office Action mailed March 17, 2005, p. 2.

In response to the arguments traversing the rejection based on Blackshear and set forth in Applicants' Response filed December 13, 2004, the Examiner stated:

> Regarding the argument that Blackshear does not teach testing of a stack of at least two semiconductor die prior to mounting on a substrate, Blackshear does teach this. Blackshear teaches pre-testing of a chip package prior to mounting on a substrate and teaches that a chip package may comprise more than one ship (die), therefore teaching testing of a stack of at least two semiconductor die prior to mounting on a substrate.

Office Action mailed March 17, 2005, p. 8.

Applicants respectfully traverse this rejection. Applicants submit that for the reasons set forth in Applicants' Response filed December 13, 2004, and for the reasons further discussed below, that Blackshear does not anticipate claims 1, 9-11, 15, 18, and 20.

First, anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be *identically* shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

Second, the prior art relied on by the Examiner in making a rejection under Section 102 must be enabling. *See In re Hoeksema*, 3999 F.2d 269, 158 U.S.P.Q. 596 (C.C.P.A. 1968). "In determining that quantum of prior art disclosure which is necessary to declare an applicant's invention 'not novel' or 'anticipated' within section 102, the stated test is whether a reference contains an 'enabling disclosure' . . . ." *Id.* The disclosure in an assertedly anticipating reference must provide an enabling disclosure of the desired subject matter; mere naming or description of the subject matter is insufficient. *Elan Pharm., Inc. v. Mayo Foundation for Medical and Education Research*, 346 F.3d 1051, 1054, 68 U.S.P.Q.2d 1373, 1376 (Fed. Cir. 2003) (holding that the disclosure must be enabling and not require undue experimentation).

Applicants again respectfully assert that the Blackshear reference fails to teach each and every element or step of the present claims. Applicants also respectfully assert that the Blackshear reference fails to enable the presently claimed subject matter.

The present application relates to an improved stacked die module and techniques for forming an improved stacked die module. Application, page 2. Specifically, techniques and embodiments disclosed in the present application address problems with existing design techniques by reducing packaging costs and potential for package damage. *See id.* at 10. In existing techniques, die are typically stacked from the surface of a substrate, requiring multiple iterations and significant handling by die attach machines. *Id.* Such die stacking equipment may be costly, slow and inaccurate. *Id.* Further, with chip design yielding increasingly thinner die, excess handling of individual die in a conventional stacking process may increase the likelihood of damage to die. *Id.* Embodiments of the present invention address these problems by forming and testing a die stack prior to attaching the die stack to a substrate. *Id.* at 12. Accordingly, independent claim 1 recites, in relevant part, "forming a stack of at least two semiconductor die; and after the stack is formed, testing the semiconductor die in the stack."

In contrast, the Blackshear reference is directed to individual memory chip packages that are pre-tested before being mounted on substrates. *See* Blackshear et al., col. 2, lines 46-48. The Examiner cited claim 14 of the Blackshear reference in an attempt to show that the Blackshear reference teaches a "*stack* [that] is tested prior to mounting on a packaging substrate." Office Action, page 2. However, independent claim 13, from which claim 14 depends, makes it clear that the Blackshear reference is directed to pre-testing of single memory chip packages, not a *stack* of *at least two* semiconductor die. In fact, claim 13 in the Blackshear reference recites "a *single* memory chip package mounted on each of said substrates." (Emphasis added). Accordingly, when claim 14 of the Blackshear reference recites that "said memory chip package comprises a pre-tested memory chip package," it is referring to a single memory chip package, not

a *stack* of semiconductor die. Thus, at most, the Blackshear reference discloses testing a "memory chip package," before stacking the packages to provide the configuration illustrated in Fig. 1 of the Blackshear reference.

Thus, as recognized by the Examiner, Blackshear teaches testing of a chip package prior to mounting on a substrate. *See* Office Action mailed March 17, 2005, p. 2; Blackshear, col. 4, ll. 8-9. The Blackshear reference further discloses that a "chip package may include one or many chips." Blackshear, col. 3, lines 53-54. However, contrary to the Examiner's assertion, Blackshear does not teach "forming a *stack* of at least two semiconductor die." (Emphasis added). For example, the chip package illustrated in FIG. 3 of Blackshear includes a chip 301 attached to a substrate 302. While the Blackshear reference makes a cursory disclosure that the chip package may include one or many chips, at no point does Blackshear show a *stack* of chips or semiconductor die. Blackshear only teaches that a chip package 300 "may include one or many chips." *See* Blackshear col. 3, ll. 52-53. There is no showing in Blackshear that a multiple chip package includes a *stack* of chips. Accordingly, at most, one of ordinary skill in the art would conclude that the multiple chip package comprises a plurality of chips assembled adjacent to one another. The Examiner's assertion that the multiple chip package of Blackshear comprises a *stack* of chips or semiconductor die is neither disclosed nor suggested by Blackshear. Accordingly, Applicants respectfully submit that the Blackshear reference *does* not disclose "forming a stack of at least two semiconductor die," as recited in claim 1. For this reason alone, the Blackshear reference cannot possibly anticipate the present claims.

Additionally, Blackshear does not *enable* "forming a stack of at least two semiconductor die." Even if the description of a multiple chip package could be reasonably interpreted to refer to a stack of at least two semiconductor die, the Blackshear reference does not *enable* "forming the stack". Blackshear discloses chip scale packages "that have been burned in and tested." *See id.* at col. 4, ll. 23-26. The multiple chip package is described as an alternative chip package that may be used in the invention, but the formation of a multiple chip package is neither discussed nor enabled. Finally, "forming a stack" of chips or semiconductor die is not illustrated in the chip package in FIG. 3. Therefore, the Blackshear reference fails to *disclose* or *enable* "forming a stack of at least two semiconductor die."

Applicants also assert that Blackshear does not disclose "testing the semiconductor die in the stack prior to attaching the semiconductor die to a packaging substrate." As noted by the Examiner, in claim 14 Blackshear recites "a pre-tested memory chip package that is tested for defects before being mounted on said substrates." As stated above, Blackshear does not teach a chip package containing a *stack* of semiconductor die. Therefore, a pre-tested memory chip package as defined by Blackshear does not disclose a tested semiconductor die *stack*. A pre-tested memory chip package, as disclosed in Blackshear, may disclose a package with multiple chips but, as discussed above, the multiple chip package disclosed does not disclose a *stack* of chips or semiconductor die.

Blackshear discloses pre-testing a memory chip package before being "mounted on said substrate." Clearly, Blackshear is referring to pre-testing the chip package 140 before mounting on the substrate 120. *See id.* at FIG. 1. Blackshear is not referring to testing the chip 301 before

mounting on the substrate 302 of the chip package. Blackshear discloses testing a chip package after the package is assembled. This package is in turn placed on another substrate 120, constructing the Blackshear invention. *See id.* at col. 3, ll. 4-8. Conversely, claim 1 of the instant application recites testing "the semiconductor die in the stack *prior* to attaching the semiconductor die to a packaging substrate." (Emphasis added). Correlating the recitation of claim 1 with Blackshear would require testing the chip 301 before mounting on the substrate 302. This is in stark contrast to the method taught by Blackshear of testing the assembled chip package 140 before mounting on the substrate 120. In addition, Blackshear notes that "the direct burn in of single chips (without chip packages) is impractical for several reasons," thus confirming that Blackshear does not teach testing a die or stack of die before attaching to the substrate of the chip package. *See id.* at col. 3, ll. 62-67; col. 4, ll. 1-7. Therefore, the Blackshear reference fails to disclose "after the stack is formed, testing the semiconductor die in the stack prior to attaching the semiconductor die to a packaging substrate," as recited in claim 1.

In view of the deficiencies discussed above and in the prior Response filed December 13, 2004, Applicants assert that the Blackshear reference fails to disclose each and every element recited in independent claim 1. Therefore, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claim 1. Further, claims 9-11, 15, 18 and 20 depend from independent claim 1. Accordingly, Applicants request withdrawal of the Examiner's rejection and allowance of claims 9-11, 15, 18 and 20 based on their respective dependencies and for the unique subject matter separately recited in each dependent claim.

Rejections under 35 U.S.C. § 103

The Examiner rejected claim 17 under 35 U.S.C. § 103(a) as being unpatentable over Blackshear in view of Huang et al.(U.S. Patent No. 6,753,206; hereinafter "Huang"). The Examiner also rejected claims 8, 12-13, 16 and 19 under 35 U.S.C. § 103(a) as being unpatentable over Jiang et al. (U.S. Patent No. 6,343,019) in view of Blackshear et al. and Pai et al. (U.S. Patent No. 6,503,776). Further, the Examiner rejected claim 14 under 35 U.S.C. § 103(a) as being unpatentable over Jiang et al. in view of Blackshear and Moden (U.S. Patent No. 5,719,440) or Hakey et al. (U.S. Patent No. 6,627,477 B1).

Applicants respectfully traverse these rejections. Applicants assert, with the considerations presented in the Response filed December 13, 2004, and further discussion below, that the cited references do not render obvious claims 8, 12-14, 16, 17 and 19.

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (Bd. Pat. App. & Inter. 1985).

Dependency on Independent Claim 1

As discussed above and in the previous Response filed December 13, 2004, with respect to the rejections under 35 U.S.C. § 102, Applicants assert that independent claim 1 is presently allowable. As discussed in detail above and in the previous Response, the Blackshear reference fails to disclose each of the elements recited in independent claim 1. For this reason alone, Applicants respectfully submit that claims 8, 12-14, 16, 17 and 19, which are dependent thereon, are also allowable. Applicants submit that neither the Jiang reference, the Pai reference, the Hakey reference, nor the Moden reference cures the deficiencies discussed above with respect to the allowable base claim. Accordingly, the cited references, taken alone or in combination, do not disclose all of the presently claimed elements. Thus, a *prima facie* case of obviousness has not been established. Applicants respectfully request withdrawal of the Examiner's rejections under 35 U.S.C. § 103 and allowance of claims 8, 12-14, 16, 17 and 19.

Dependent Claim 17

Further, while Applicants submit that claim 17 is allowable based on its dependency to claim 1, Applicants further submit that claim 17 is also allowable for the subject matter separately recited therein. Claim 17 recites a method of testing semiconductor die wherein "the act of forming comprises forming a shingle stack." As described in the present specification, as amended, FIGs. 5C and 5D are cross-sectional views of "shingle stacks." *See* Application, Page 14, line 15. Shingle stacks are die stacks wherein upper die may overhang die below them in the stack such that their centers are not aligned. *See id.* at Page 14, lines 17-18. Contrary to the Examiner's assertion, Huang does not disclose a shingle stack as reasonably interpreted in light of

the present specification. That is to say that Huang does not disclose a die stack wherein an upper die overhangs a lower die. Even if the integrated circuit package disclosed in Huang could be fairly characterized as a die stack, the upper die does not overhang the die below. The upper die does not "overhang" anything. As clearly illustrated in FIG. 2 of Huang, the upper die is adhered directly and completely to a lead frame. Thus, no portion of the upper die overhangs anything. Accordingly, none of the cited references, either alone or in combination, discloses all of the features recited in claim 17.

Because the cited references, taken alone or in combination, fail to disclose each of the features recited in claim 17, Applicants respectfully submit that the cited combination cannot possibly render the recited subject matter obvious. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejections and allowance of claim 17.

Conclusion

In view of the remarks set forth above, Applicants respectfully request reconsideration of the Examiner's rejections and allowance of all pending claims. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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